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Notice of Allowability	Application No.	Applicant(s)	
	10/674,044	CALLAGHAN, DAVID M.	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 23 August 2007*.

2. ☒ The allowed claim(s) is/are *1,2,4,5,7-24,26-28 and 30-43*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1, 2, 4, 5, 7-24, 26-28, and 30-43 are allowed.

Response to Arguments

2. Applicant's arguments, see page 10 of amendment, filed 23 August 2007, with respect to claim 42 have been fully considered and are persuasive. The 35 U.S.C. 101 rejection of claim 42 has been withdrawn.

3. Applicant's arguments, see page 10 of amendment, filed 23 August 2007, with respect to claims 30 and 34 have been fully considered and are persuasive. The 35 U.S.C. 112(2) rejections of claims 30 and 34 have been withdrawn.

4. The following is an examiner's statement of reasons for allowance:

5. Referring to claim 1, 2, 4, 5, 7-13, and 43, the prior art does not teach "the self-testing RAM interface with the memory array and a central processing unit (CPU) of the computer are formed on separate integrated circuits and the self-testing RAM interface cooperates with the CPU to facilitate testing memory array data cells by dividing the memory array, so that each of the CPU and the microprocessor concurrently test the array thus facilitating faster testing of the memory array."

6. Referring to claims 14-19, the prior art does not teach "a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit boards; the self-testing RAM interface subsystem cooperates with the CPU to facilitate testing memory storage banks by dividing the memory storage banks, so that the CPU and the microprocessor concurrently test the memory storage banks thus facilitating faster testing of the memory storage bank."

7. Referring to claims 20 and 21, the prior does not teach "wherein the memory cells store copies of the input data and the self-testing interface cooperates with the CPU to facilitate testing memory stores by dividing the memory stores, so that each of the CPU and the microprocessor concurrently test the stores thus facilitating faster testing of the memory stores."

8. Referring to claims 22-24, 26, and 27, the prior art does not teach "testing the one or more memory cells by dividing the memory cells, so that the CPU and the self testing RAM interface concurrently test the cells thus facilitating faster testing of the memory cells."

9. Referring to claim 28, the prior art does not teach "embedding a second microprocessor in a single circuit board with the memory device, the CPU and the

memory device are formed of different integrated circuits; and dividing memory cells on the memory device so that the CPU and the second microprocessor concurrently test the cells thus facilitating faster testing of the memory cells."

10. Referring to claim 30-33, the prior does not teach "facilitating faster detection of hard errors by dividing the memory cells, so that the CPU and the microprocessor concurrently test the cells."

11. Referring to claim 34-42, the prior does not teach "dividing a memory device including the memory address, so that each of the CPU and the microprocessor concurrently test the memory device".

12. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
September 14, 2007